

WHAT IS CLAIMED IS:

1 1. A circuit arrangement for adding a first binary operand of N bits and a second binary
2 operand of M bits, N being greater than or equal to M, comprising:
3 an adder adapted to add representative sets of least-significant bits of the first and
4 second binary operands together to produce a least-significant bits partial sum and a carryout;
5 and
6 a multiplexer circuit coupled to the adder and adapted to output a most-significant bits
7 partial sum by passing one of: a representative set of most-significant bits of the first binary
8 operand, and an offset of the representative set of most-significant bits of the first binary
9 operand, responsive to selection data, the selection data being a function of the most-
10 significant bit of the representative set of least-significant bits of the first binary operand.

1 2. The circuit arrangement of claim 1, wherein the adder is an M-bit adder, the
2 representative sets of least-significant bits of the first and second binary operands each have a
3 length of M bits, and the selection data includes a carryout from the M-bit adder, and the Mth
4 bit of the first binary operand.

1 3. The circuit arrangement of claim 2, wherein the N-M bit most-significant bits partial
2 sum is one of: the N-M most significant bits of the first binary operand, the N-M most
3 significant bits of the first binary operand incremented by one, and the N-M most significant
4 bits of the first binary operand decremented by one.

1 4. The circuit arrangement of claim 3, wherein N is 24 and M is 16.

1 5. The circuit arrangement of claim 1, wherein the offset of the representative set of
2 most-significant bits of the first binary operand include a first incremented offset, and a
3 second decremented offset.

1 6. The circuit arrangement of claim 5, wherein the first incremented offset is the
2 representative set of most-significant bits of the first binary operand incremented by one, and
3 the second incremented offset is the representative set of most-significant bits of the first
4 binary operand decremented by one.

1 7. The circuit arrangement of claim 6, wherein the multiplexer circuit includes a
2 multiplexer adapted to select one of at least three input binary quantities.

1 8. The circuit arrangement of claim 1, wherein the selection data includes the most-
2 significant bit of the representative set of least-significant bits of the first binary operand, and
3 a carryout from the adder.

1 9. The circuit arrangement of claim 8, wherein the carryout is available from the adder
2 before the least-significant bits partial sum.

1 10. The circuit arrangement of claim 1, wherein the offset of the representative set of
2 most-significant bits of the first binary operand include a first incremented offset, and a
3 second decremented offset, wherein the first incremented offset is the representative set of
4 most-significant bits of the first binary operand incremented by one, and the second
5 incremented offset is the representative set of most-significant bits of the first binary operand
6 decremented by one, wherein the selection data includes the most-significant bit of the
7 representative set of least-significant bits of the first binary operand, and a carryout from the
8 adder, and wherein the carryout is available from the adder before the least-significant bits
9 partial sum.

1 11. The circuit arrangement of claim 1, wherein N-M is one, and the multiplexer circuit is
2 further configured to operate as an exclusive-or gate, the selection data being the most-
3 significant bit of the first binary operand and a carryout from the adder.

8 data being a function of the most-significant bit of the representative set of least-significant
9 bits of the first binary operand.

1 19. A circuit arrangement for adding a first binary operand of N bits and a second binary
2 operand of M bits, N being greater than or equal to M, comprising:
3 means for adding representative sets of least-significant bits of the first and second
4 binary operands together to produce a least-significant bits partial sum and a carryout; and
5 means for outputting a most-significant bits partial sum by passing one of: a
6 representative set of most-significant bits of the first binary operand, and an offset of the
7 representative set of most-significant bits of the first binary operand, responsive to selection
8 data, the selection data being a function of the most-significant bit of the representative set of
9 least-significant bits of the first binary operand.

1 20. A computer-implemented method for adding M most-significant bits of a first N-bit
2 binary operand and M most-significant bits of a second N-bit binary operand, comprising:
3 an adder adapted to add representative sets of least-significant bits of the first and
4 second binary operands together to produce a N-M+1 bit partial sum ;
5 a first multiplexer circuit coupled to the adder and adapted to produce an output
6 representative of the adder's (N-M)th bit internal carry bit, responsive to a first selection data
7 set, the first selection data set including each of the respective (N-M+1)th bits of the binary
8 operands, and the (N-M+1)th bit of the partial sum; and
9 a second multiplexer circuit coupled to the first multiplexer circuit and adapted to
10 output an most-significant bits partial sum by passing one of: a representative set of most-
11 significant bits of the second binary operand, and an offset of the representative set of most-
12 significant bits of the second binary operand, responsive to the first multiplexer output.